AMENDMENTS TO THE CLAIMS

1. (Original) A data bus system that has an input/output (I/O) unit, a central processing unit (CPU), an internal memory unit, and a peripheral circuitry, the data bus system comprising:

an external access bus used when data is output from the CPU or data is input to the I/O unit or the internal memory unit;

an internal access bus used when data is input to the CPU, data is output from the I/O unit or the internal memory unit, or data is input to or output from the peripheral circuitry; and

an internal memory test bus used when data is output from the internal memory unit and input to the I/O unit, wherein

the CPU is connected to an external access bus and an internal access bus:

the internal memory unit is connected to the external access bus, the internal access bus and a test bus;

the I/O unit is connected to the external access bus, the internal access bus and the test bus;

the periphery circuitry is connected only to the internal access bus;

the internal access bus is connected to the external access bus with a latch; and

the data bus system can access all of an internal/external memory, an external porter and internal periphery circuits, and can also access an internal memory test mode using a read only internal memory test bus.

2. (Original) The data bus system of claim 1, wherein the external and internal access buses are constructed to have a latch structure so as to be connected to each other.

3. (Currently Amended) The data bus system of claim 1, further comprising:

a CPU read bus which acts as a path of the movement of data between the CPU and the internal access bus;

a first three-phase buffer which is enabled in response to a CPU read signal and enabling data to move via the CPU read bus;

a CPU write bus which acts as a path of the movement of data between the CPU and the external access bus; and

a second three-phase ~~bus~~ buffer which is enabled in response to a CPU write signal and enabling data to move via the CPU write bus.

4. (Original) The data bus system of claim 1, further comprising:

an internal memory read control block which is positioned between the internal memory unit and the internal access bus in order to read data in the internal memory unit; and

an internal memory write control block which is positioned between the internal memory unit and the external access bus in order to write data to the internal memory unit.

5. (Original) The data bus system of claim 1, further comprising:

a peripheral circuitry read bus that acts as a path of the movement of data from the peripheral circuitry to the internal access bus;

a third three-phase buffer that is enabled in response to a peripheral circuitry read signal and enabling data to move via the peripheral ciruitry read bus;

a peripheral circuitry write bus which acts as a path of the movement of data from the internal access bus to the peripheral circuitry; and

6. (Currently Amended) The data bus system of claim 1, further comprising a fifth three-phase buffer which is enabled in response to a predetermined enable signal and enabling data to be moved between the internal memory unit ~~an~~ and the internal memory test bus.

7. (Original) The data bus system of claim 6, wherein the enable signal is an output signal output from an AND gate when an internal memory access enable signal, a test mode signal, and an internal memory access signal are input to the AND gate.

8. (Original) The data bus system of claim 7, wherein the internal memory access enable signal is generated in synchronization with a system clock, and the data in the internal memory unit is dumped in synchronization with a rising edge of the internal memory access enable signal.

9. (Original) The data bus system of claim 1, further comprising:

a data port used to transmit external data;

a data port control block which controls data in the data port; and

an external data bus which acts as a path of the movement of data among the data port, the data port control block, and the external access bus.

10. (Original) The data bus system of claim 9, further comprising a sixth three-phase buffer which is enabled in response to a predetermined enable signal and enabling data to be moved from the internal memory test bus to the data port control block.

11. (Original) The data bus system of claim 10, wherein the enable signal is an output signal output from the AND gate when a test mode signal and an internal memory enable signal are input to the AND gate.

12. (Original) The data bus system of claim 9, further comprising:

a seventh three-phase buffer which is enabled in response to an external data write signal and enabling data to be moved from the internal access bus to the data port control block; and

an eighth three-phase buffer which is enabled in response to an internal memory read signal and enabling data to be moved from the internal access bus to the data port control block.

13. (Original) The data bus system of claim 9, further comprising a ninth three-phase buffer which is enabled in response to a predetermined enable signal and enables data to be moved from the data port to the external access bus.

14. (Original) The data bus system of claim 13, wherein the enable signal is an output signal output from an OR gate when an internal memory write signal , an external data read signal, and an internal memory read signal are input to the OR gate.